

ISL85415EVAL2Z Wide V_{IN} Negative V_{OUT} Sync Buck-Boost Regulator up to 500mA

Description

The ISL85415EVAL2Z kit is intended for use for point-of-load applications sourcing from 3V to 36V. The kit is used to demonstrate the performance of the ISL85415 wide V_{IN} low quiescent current high efficiency sync buck regulator in negative output configuration with up to 500mA output current.

The ISL85415 is offered in a 4mmx3mm 12 Ld DFN package with 1mm maximum height. The converter occupies 2.418cm² area.

Specifications

This board has been configured and optimized for the following operating conditions:

- V_{IN} = 3V to 31V
- V_{OUT} = -5V
- I_{MAX} = 700mA (at V_{IN} = 31V)
- Peak efficiency: >85.6% at 250mA, V_{IN} = 12V
- Board temperature: +25°C

References

[ISL85415](#) Datasheet

Key Features

- Wide input voltage range 3V to 36V
- Synchronous operation for high efficiency
- Integrated high-side and low-side NMOS devices
- Programmable switching frequency (fixed or externally synchronized)
- Continuous output current up to 500mA (refer to [Figure 7](#))
- Internal or external soft-start
- Minimal external components required
- Power-good and enable functions available
- On-board jumper for selecting PFM or forced PWM at light loads
- On-board EN switch

Recommended Equipment

The following materials are recommended to perform testing:

- 0V to 50V power supply with at least 2A source current capability
- Electronic loads capable of sinking current up to 1.5A
- Digital Multimeters (DMMs)
- 100MHz quad-trace oscilloscope

Ordering Information

PART NUMBER	DESCRIPTION
ISL85415EVAL2Z	Wide V_{IN} (3V-31V) Negative V_{OUT} Sync Buck-Boost Integrated FET Regulator up to 500mA

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TABLE 1. EXTERNAL COMPONENT SELECTION

V _{OUT} (V)	L ₁ (μH)	C ₅ +C ₆ (μF)	R ₁ (kΩ)	R ₂ (kΩ)	C ₄ (pF)	R _{FS} (kΩ)	R ₃ (kΩ)	C ₇ (pF)
-12	45	10	90.9	4.75	22	115	51.1	470
-5	22	2x22	90.9	12.4	100	120	51.1	470
-3.3	22	2x22	90.9	20	100	120	51.1	470

PCB Layout Guidelines

The ISL85415EVAL2Z PCB layout has been optimized for electrical and thermal performance. Proper layout of the power converter will minimize EMI and noise while insuring first pass success of the design.

PCB layouts are provided in multiple formats on the Intersil web site. In addition, [Figures 3 to 6](#) will clarify the important points in PCB layout. In reality, PCB layout of the ISL85415EVAL2Z is quite simple.

A multi-layer printed circuit board with GND plane is recommended. [Figure 3](#) shows the connections of the critical components in the converter. The most critical connections are to tie the PGND pin to the package GND pad and then use vias to directly connect the GND pad to the system GND plane. This connection of the GND pad to system plane insures a low impedance path for all return current, as well as an excellent thermal path to dissipate heat.

With this connection made, place the high frequency MLCC input capacitors C₁, C₂ near the VIN pin and use vias directly at the capacitor pads to tie the capacitors to the system GND plane. Also use vias directly at the C₅, C₆ output capacitor pads to tie the capacitors to the system GND plane. These measures will minimize the high dV/dt and dI/dt loops.

Minimize the PHASE connection by placing L₁ close to the IC and on the same side. Place the BOOT capacitor (C₃) very close to the IC.

Place a 1μF MLCC near the VCC pin and directly connect its return with a via to the system GND plane.

Keep the power components path (L₁, C₁, C₂, C₃, C₅, C₆) separated from the small signal nodes (FB, COMP) and the control components path (FS, SS) by placing the feedback divider close to the FB pin and do not route any feedback components near PHASE or BOOT. If external components are used for SS, COMP or FS, the same advice applies. Connect these control components and small signal noise components to system GND.

Keep the small signal nodes traces (FB, COMP) as short as possible.

Quick Setup Guide

1. Ensure that the circuit is correctly connected to the supply and loads prior to applying any power.
2. Connect the bias supply to VIN, the plus terminal to VIN (P4) and the negative return to GND (P5).
3. Verify that the position is ON for SW1.
4. Turn on the power supply.
5. Verify the output voltage is -5V for -V_{NEG} (P7).

Evaluating the Other Output Voltages

The ISL85415VAL1Z kit output is preset to -5V, however the output can be adjusted from -3.3V to -12V. The output voltage programming resistor, R₂, will depend on the desired output voltage of the regulator and the value of the feedback resistor R₁, as shown in [Equation 1](#).

$$R_2 = R_1 \left(\frac{0.6}{V_{OUT} - 0.6} \right) \quad (\text{EQ. 1})$$

[Table 1](#) shows the component selection that should be used for the respective V_{OUTS} of -3.3V, -5V and -12V.

The curves in [Figure 7](#) indicate the maximum output current the converter can deliver as a function of the input voltage and the selected output voltage configuration.

[Figures 8, 9](#) and [10](#) show the efficiency for different input voltage, output voltage and load combinations. [Figures 11, 12](#) and [13](#) show the output regulation with load while [Figures 14, 15](#) and [16](#) show the output regulation with input voltage, for different output voltages. [Figures 17 to 21](#) show some performance curves of the board during start-up, shutdown, steady state, and load transient.

Frequency Control

The ISL85415 has an FS pin that controls the frequency of operation. Programmable frequency allows for optimization between efficiency and external component size. It also allows low frequency operation for low V_{OUTS} when minimum on time would limit the operation otherwise. Default switching frequency is 500kHz when FS is tied to V_{CC} (R₁₀ = 0). By removing R₁₀, the switching frequency could be changed from 300kHz (R₁₂ = 340k) to 2MHz (R₁₂ = 32.4k). Please refer to the [ISL85415](#) datasheet for calculating the value of R₁₀. Do not leave this pin floating.

Disabling/Enabling Function

The ISL85415EVAL2Z evaluation board contains a SW1 switch that enables or disables the part, thus allowing low quiescent current state. [Table 2](#) details this function.

TABLE 2. SWITCH SETTINGS

SW1	ON/OFF CONTROL
ON	Enable V _{OUT}
OFF	Disable V _{OUT}

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SYNC Control

The ISL85415EVAL2Z evaluation board has a SYNC pin that allows external synchronization frequency to be applied. Default board configuration has $R_6 = 200k$ to V_{CC} , which defaults to PWM operation mode and also to the pre-selected switching frequency set by R_{12} (see datasheet and previous section "[Frequency Control](#)" on page 2 for details). If this pin is tied to

GND the IC will operate in PFM mode. JP1 switch allows to force the PFM or PWM modes.

Soft-Start /COMP Control

R_{15} selects between internal ($R_{15} = 0$) and external soft-start. R_{11} selects between internal ($R_{11} = 0$) and external compensation. Please refer to the Pin Description Table (Page 3) of the [ISL85415](#) datasheet.

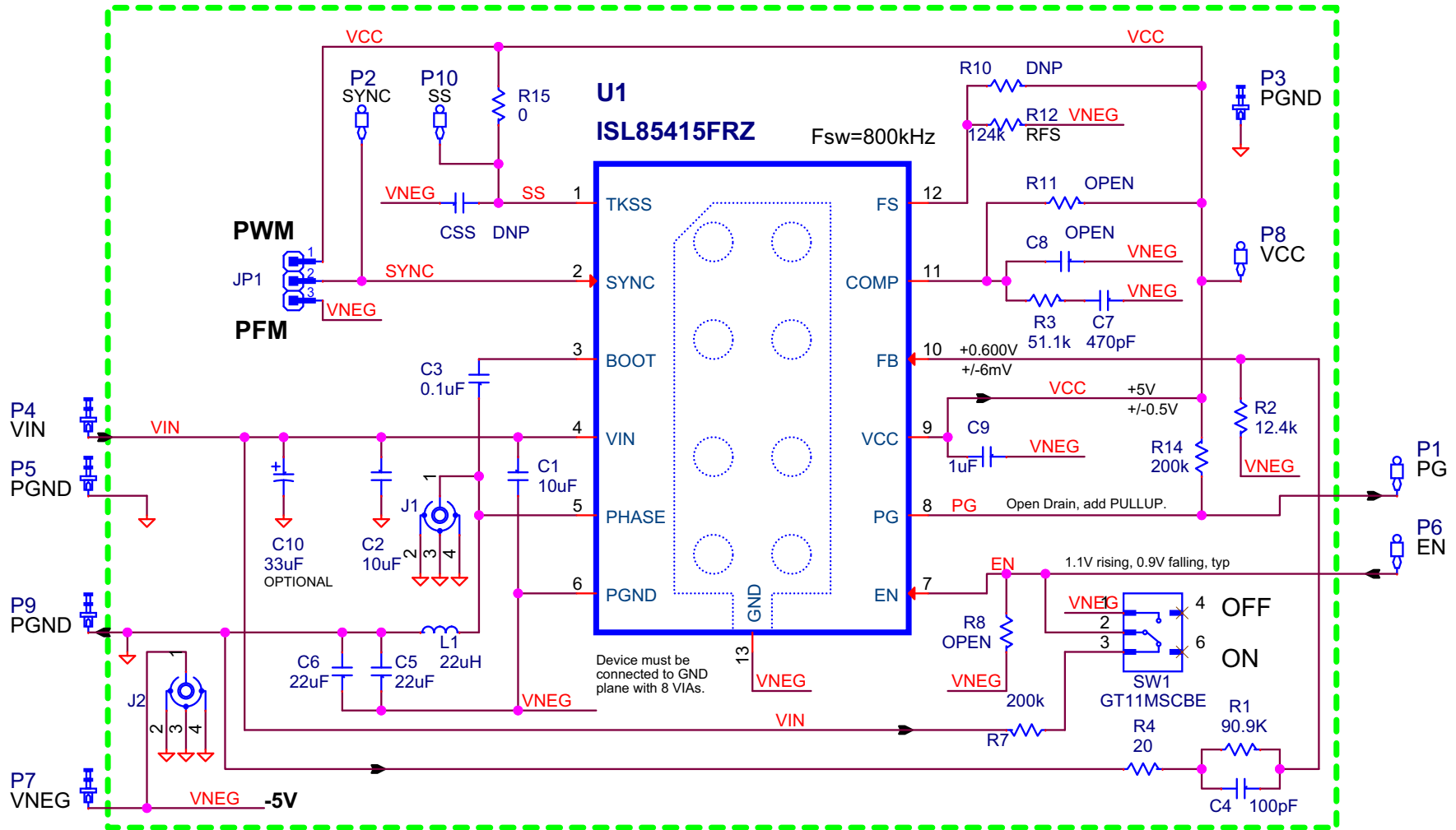


FIGURE 1. FRONT OF EVALUATION BOARD ISL85415EVAL2Z



FIGURE 2. BACK OF EVALUATION BOARD ISL85415EVAL2Z

ISL85415EVAL2Z Schematic



NOTE: The input electrolytic capacitor C₁₀ is optional and it is used to prevent transient voltages when the input test leads have large parasitic inductance. It can be removed if the IC is used in a system application.

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ISL85415EVAL2ZA Bill of Materials

PART NUMBER	QTY	REF-DES	DESCRIPTION	MANUFACTURER
ISL85415EVAL2ZREVAPCB	1	N/A	PCB - ISL85415 NEGATIVE VOUT EVALUATION BOARD	INTERSIL
EEV-HA1H330UP/PCE3303CT-ND	1	C10	Capacitor Elect 33µF 50V CASE SMD	PANASONIC/DIGIKEY
H1045-00101-50V5-T	1	C4	CAP, SMD, 0603, 100pF, 50V, 5%, COG, ROHS	PANASONIC
H1045-00104-50V10-T	1	C3	CAP, SMD, 0603, 0.1µF, 50V, 10%, X7R, ROHS	AVX
H1045-00105-16V10-T	1	C9	CAP, SMD, 0603, 1µF, 16V, 10%, X5R, ROHS	MURATA
H1045-00471-50V5-T	1	C7	CAP, SMD, 0603, 470pF, 50V, 5%, NPO, ROHS	PANASONIC
H1065-00106-50V10-T	2	C1, C2	CAP, SMD, 1206, 10µF, 50V, 10%, X5R, ROHS	TDK
H1065-00226-6R3V20-T	2	C5, C6	CAP, SMD, 1206, 22µF, 6.3V, 20%, X5R, ROHS	PANASONIC
131-4353-00	2	J1, J2	CONN-SCOPE PROBE TEST PT, COMPACT, PCB MNT	TEKTRONIX
68000-236LF	1	JP1	CONN HEADER 3POS VERT, 100 GOLD	TYCO ELECTRONICS
1514-2	5	P4, P5, P3, P7, P9	CONN-TURRET, TERMINAL POST, TH	KEYSTONE
5002	5	P1, P2, P6, P8, P10	CONN-MINI TEST POINT, VERTICAL, WHITE	KEYSTONE
H2511-00200-1/10W1-T	1	R4	RES, SMD, 0603, 20Ω, 1/10W, 1%, TF, ROHS	PANASONIC
H2511-00R00-1/10W-T	1	R15	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	VENKEL
CR0603-10W-5112FT	1	R3	RES, SMD, 0603, 51.1k, 1/10W, 1%, TF, ROHS	VENKEL
RC0603FR-0712K4L	1	R2	RES, SMD, 0603, 12.4k, 1/10W, 1%, TF, ROHS	YAGEO
H2511-09092-1/10W1-T	1	R1	RES, SMD, 0603, 90.9k, 1/10W, 1%, TF, ROHS	PANASONIC
H2511-01203-1/10W1-T	1	R12	RES, SMD, 0603, 120k, 1/10W, 1%, TF, ROHS	VISHAY/DALE
GT11MSCBE	1	SW1	SWITCH-TOGGLE, SMD, 6PIN, SPDT, 2POS, ON-ON	ITT INDUSTRIES/C and K DIVISION
DR73-220-R	1	L1	COIL-PWR INDUCTOR, SMD, 7.6mm, 22µH, 20%, 1.62A, ROHS	COOPER/COILTRONICS
ISL85415FRZ	1	U1	IC-500mA BUCK REGULATOR, 12P DFN 3X4	INTERSIL
H1045-DNP	1	C8	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS	DNI
H2511-DNP	3	R8, R10, R11	RES, SMD, 0603, DNP-PLACE HOLDER, ROHS	DNI
H1045-DNP	1	CSS	CAP, SMD, 0603, 33000pF, 16V, 10%, X7R, ROHS	DNI
LABEL-RENAME BOARD	1		ISL85415EVAL2Z.	

ISL85415EVAL2Z Board Layout

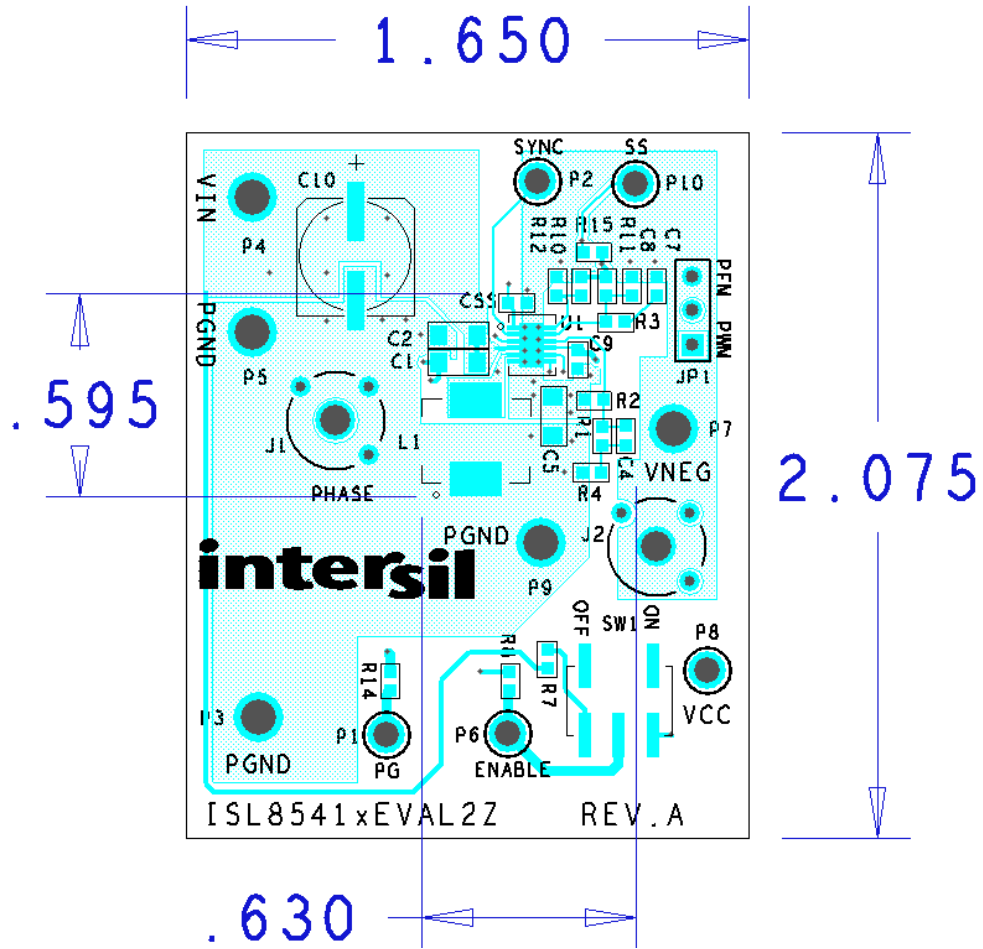


FIGURE 3. TOP

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ISL85415EVAL2Z Board Layout (Continued)

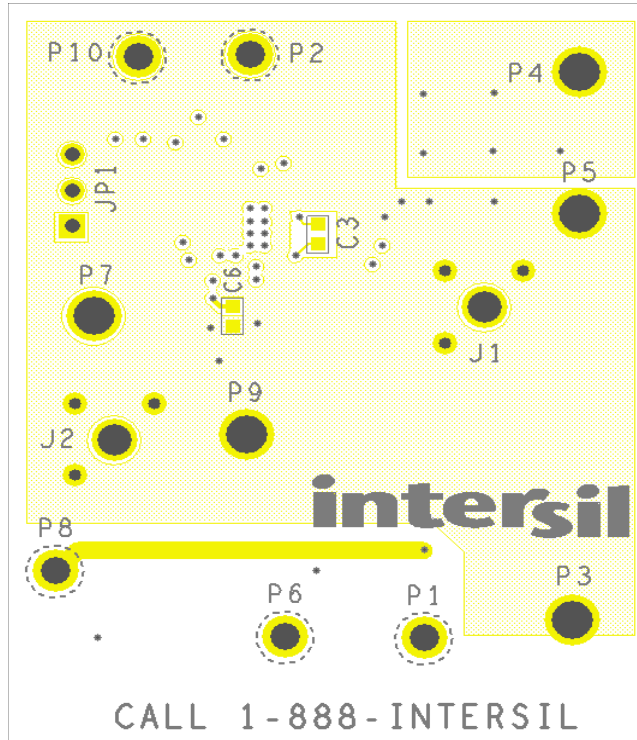


FIGURE 4. BOTTOM

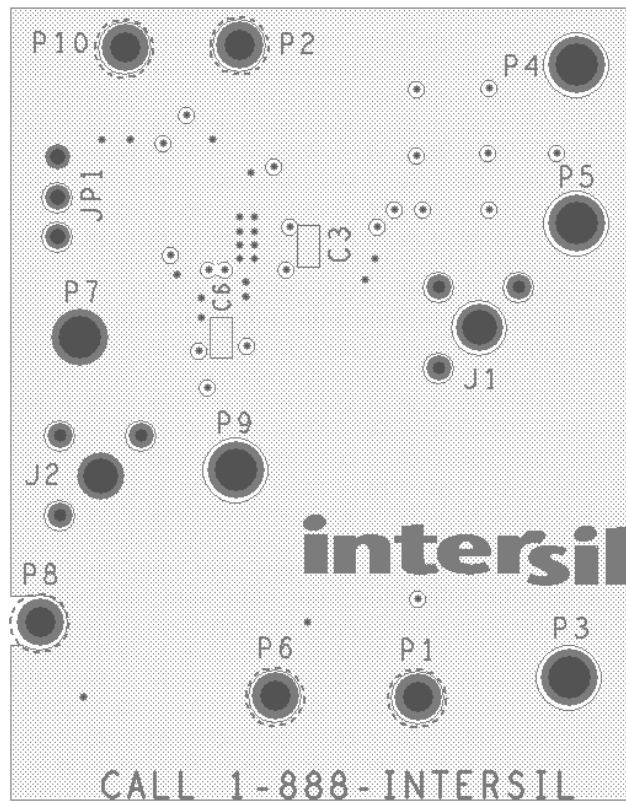


FIGURE 5. LAYER 2

ISL85415EVAL2Z Board Layout (continued)

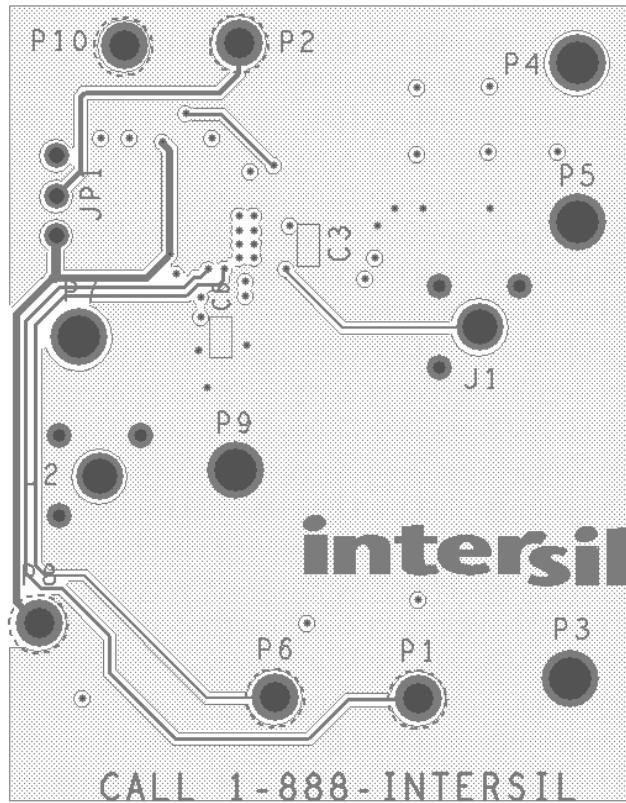


FIGURE 6. LAYER 3

Typical Performance Curves

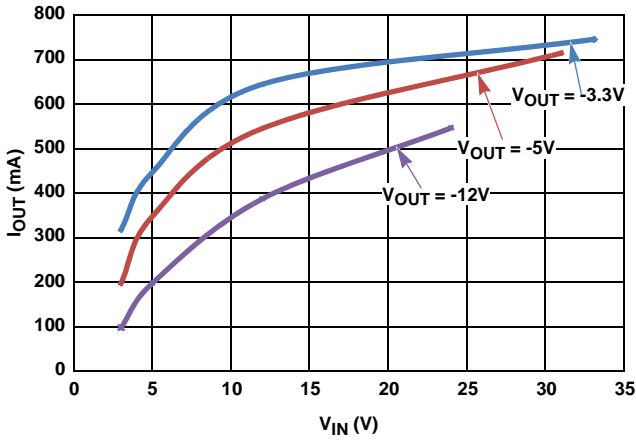


FIGURE 7. MAXIMUM I_{OUT} vs V_{IN} , $-V_{OUT}$

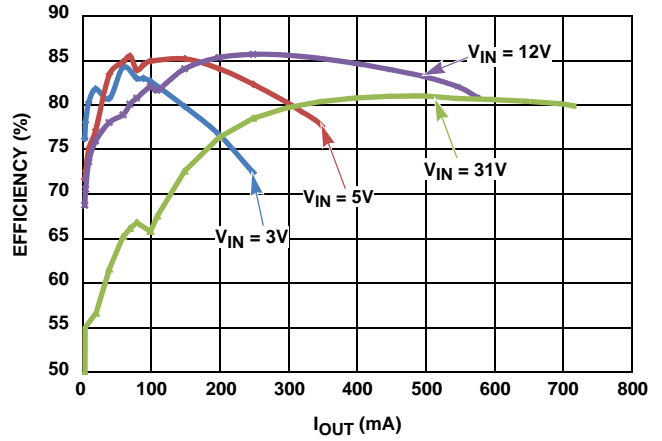


FIGURE 8. PFM EFFICIENCY, $V_{OUT} = -5V$

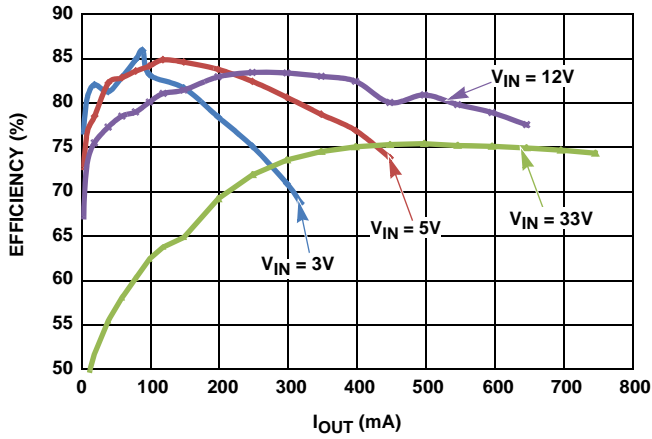


FIGURE 9. PFM EFFICIENCY, $V_{OUT} = -3.3V$

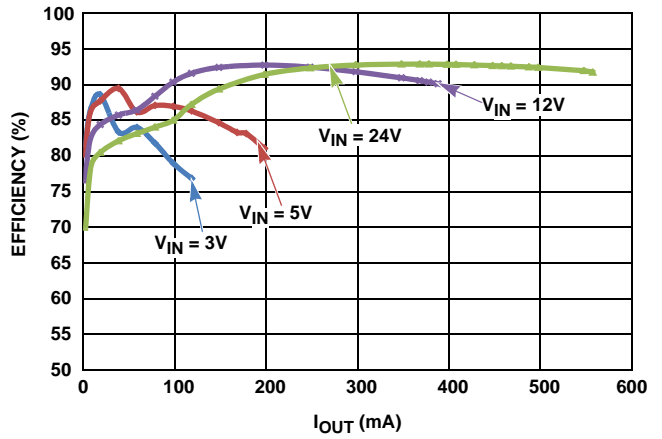


FIGURE 10. PFM EFFICIENCY, $V_{OUT} = -12V$

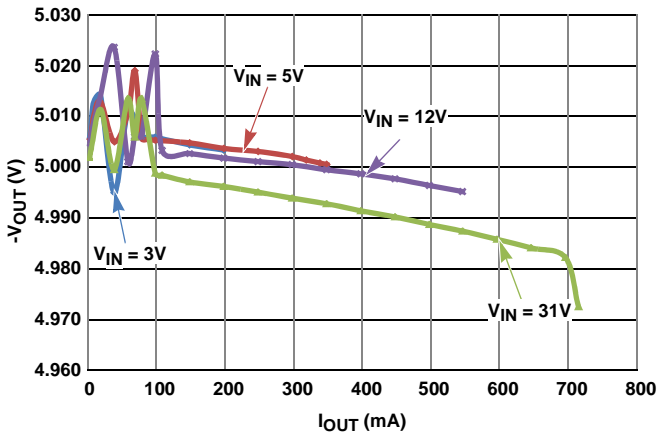


FIGURE 11. PFM LOAD REGULATION, $V_{OUT} = -5V$

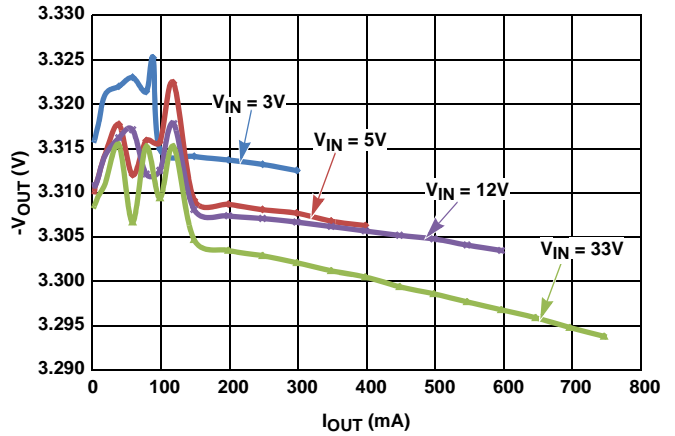


FIGURE 12. PFM LOAD REGULATION, $V_{OUT} = -3.3V$

Typical Performance Curves (Continued)

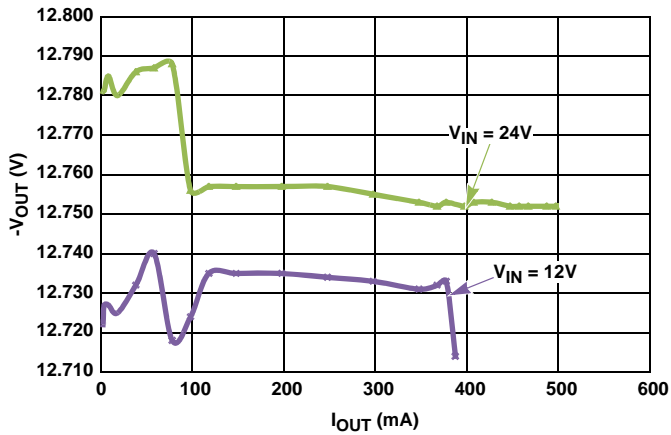


FIGURE 13. PFM LOAD REGULATION, $V_{OUT} = -12V$

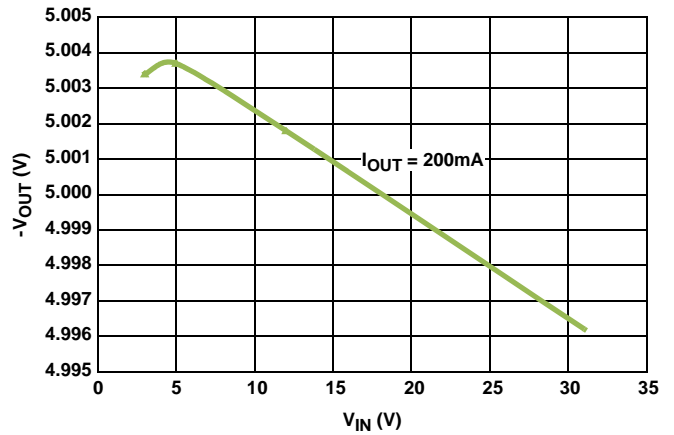


FIGURE 14. PFM LINE REGULATION, $V_{OUT} = -5V$, $I_{OUT} = 200mA$

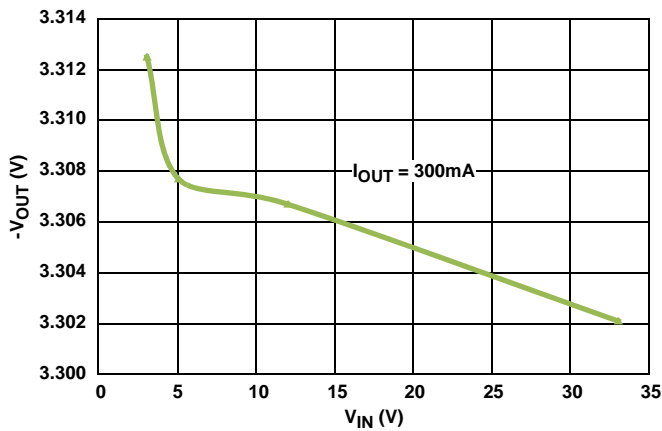


FIGURE 15. PFM LINE REGULATION, $V_{OUT} = -3.3V$, $I_{OUT} = 300mA$

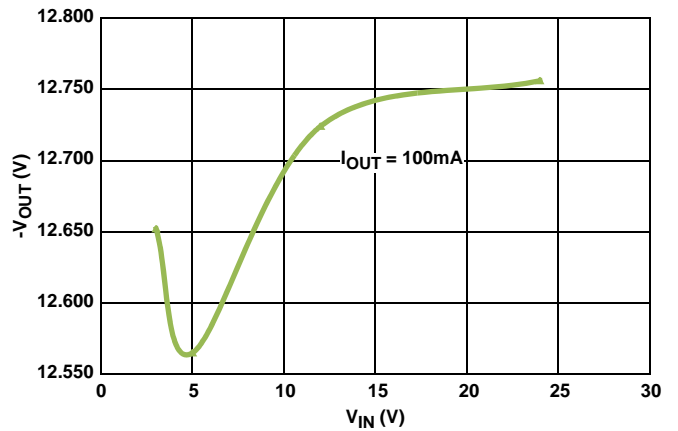


FIGURE 16. PFM LINE REGULATION, $V_{OUT} = -12V$, $I_{OUT} = 100mA$

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Typical Performance Curves $V_{IN} = 24V, V_{OUT} = -5V, \text{MODE} = \text{PWM}, \text{FSW} = 800\text{kHz}, T_A = +25^\circ\text{C}$

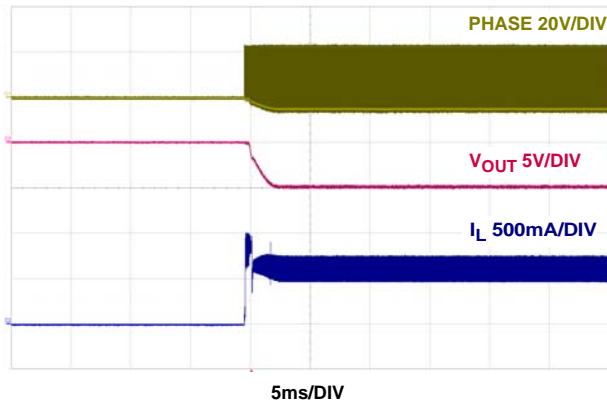


FIGURE 17. START-UP AT 500mA

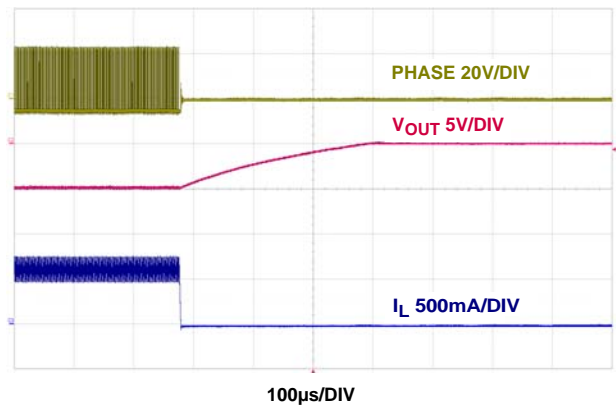


FIGURE 18. SHUTDOWN AT 500mA

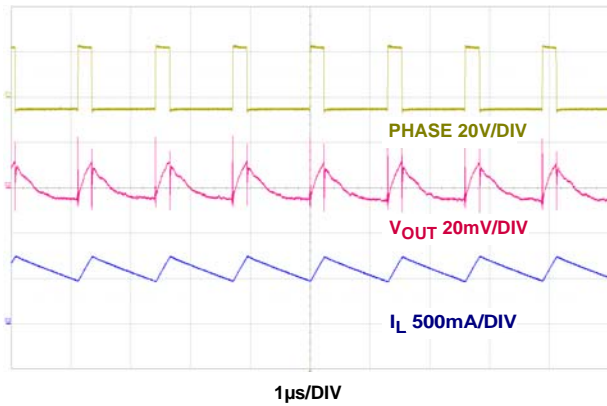


FIGURE 19. STEADY STATE AT 500mA LOAD

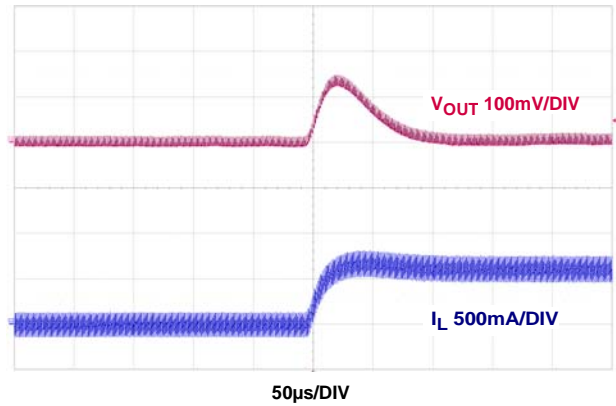


FIGURE 20. LOAD TRANSIENT

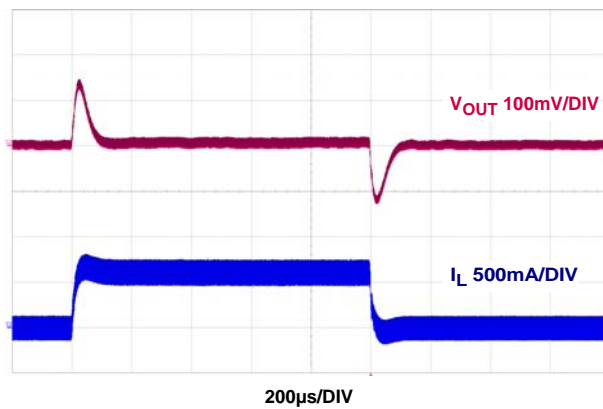


FIGURE 21. LOAD TRANSIENT

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